H04N 5/445

AF

PCT

国際事務局

特許協力条約に基づいて公開された国際出願

Recherche

(51) 国際特許分類6
H04N 5/20

A1

(11) 国際公開番号 WO99/21355

(43) 国際公開日 1999年4月29日(29.04.99)

Rec.

(21) 国際出願番号 PCT/JP98/04747

(22) 国際出願日 1998年10月20日(20.10.98)

(30) 優先権データ
特願平9/287050 1997年10月20日(20.10.97) JP
特願平10/88958 1998年4月1日(01.04.98) JP

(71) 出願人（米国を除くすべての指定国について）
ソニー株式会社(SONY CORPORATION)[JP/JP]
〒141-0001 東京都品川区北品川6丁目7番35号
Tokyo, (JP)
(72) 発明者；および
(75) 発明者／出願人（米国についてのみ）
梅村純治(UMEMURA, Shunji)[JP/JP]
佐藤一郎(SATO, Ichiro)[JP/JP]
清水克浩(SHIMIZU, Katsuhiro)[JP/JP]
〒141-0001 東京都品川区北品川6丁目7番35号
ソニー株式会社内 Tokyo, (JP)
(74) 代理人
弁理士 松隈秀盛(MATSUKUMA, Hidemori)
〒160-0023 東京都新宿区西新宿1丁目8番1号
新宿ビル Tokyo, (JP)

(81) 指定国 CN, KR, US, 欧州特許 (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

添付公開書類
国際調査報告書

(54)Title: DISPLAY DEVICE, MARKER SIGNAL FORMING METHOD, MARKER SIGNAL DETECTION CIRCUIT AND CONTROL SIGNAL GENERATION CIRCUIT

(54)発明の名称 表示装置、マーカー信号構成方法、マーカー信号検出回路、及び制御信号発生回路

combinable

(57) Abstract

A display device suitably used when a screen is divided into a plurality of areas and display comprising images having different image qualities in divided areas is effected, a marker signal forming method, a marker signal detection circuit and a control signal generation circuit. A predetermined signal pattern serving as a marker signal is provided to an image signal in an arbitrary designated area. The marker signals are disposed at both end portions in a horizontal direction in such a manner as to continue in a vertical direction, for example. The display device detects an area by detecting a marker signal and controls sharpness, contract, etc., for each detected area. In this way, image quality of the images such as a photo, a moving image, etc., can be improved without making information such as characters, numerals etc., more difficult to watch.

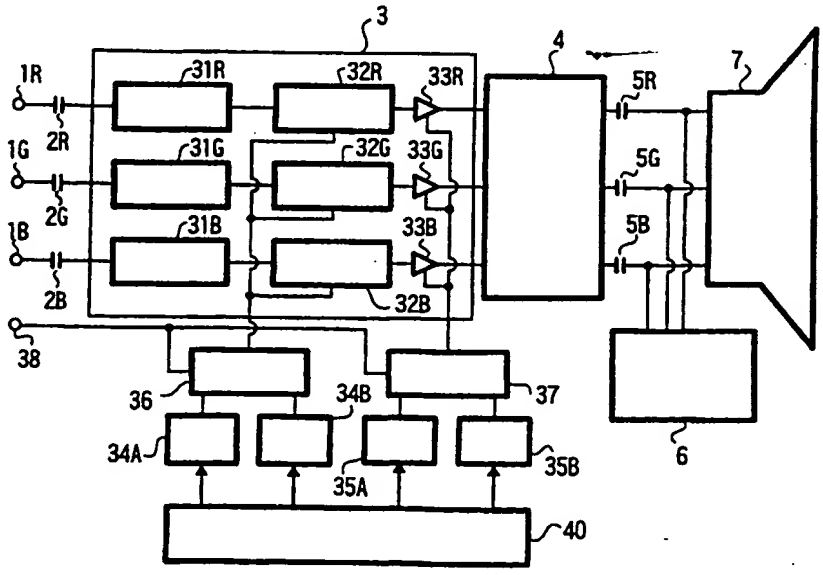


FIG. 1

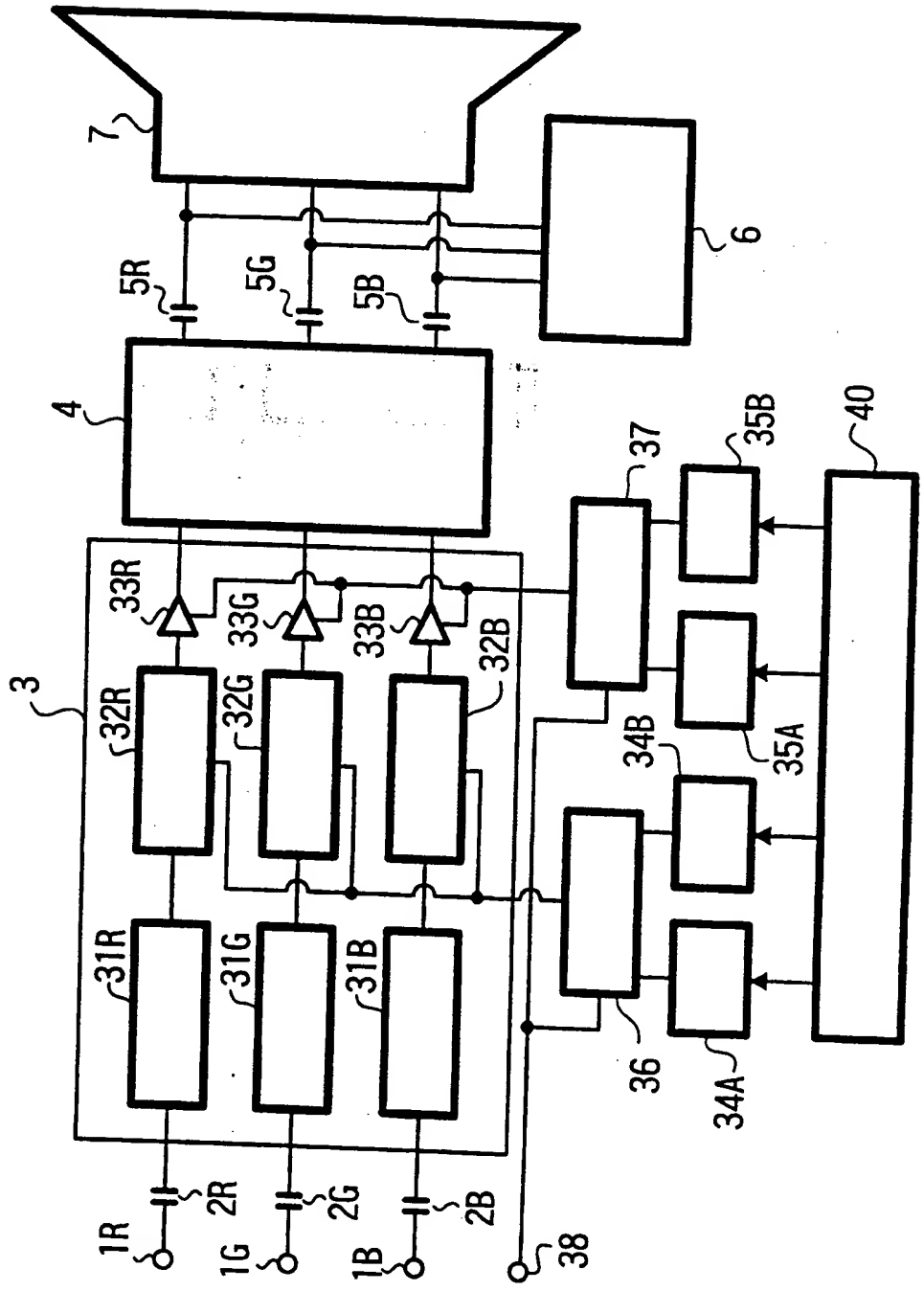

7
6
5R
5G
5B
4
3
33R
33G
33B
32B
32R
32G
31R
31G
31B
37
35B
40
34B
35A
36
34A
1R
2R
1G
2G
1B
2B
38

FIG. 2C

FIG. 2A

FIG. 2B

FIG. 2C

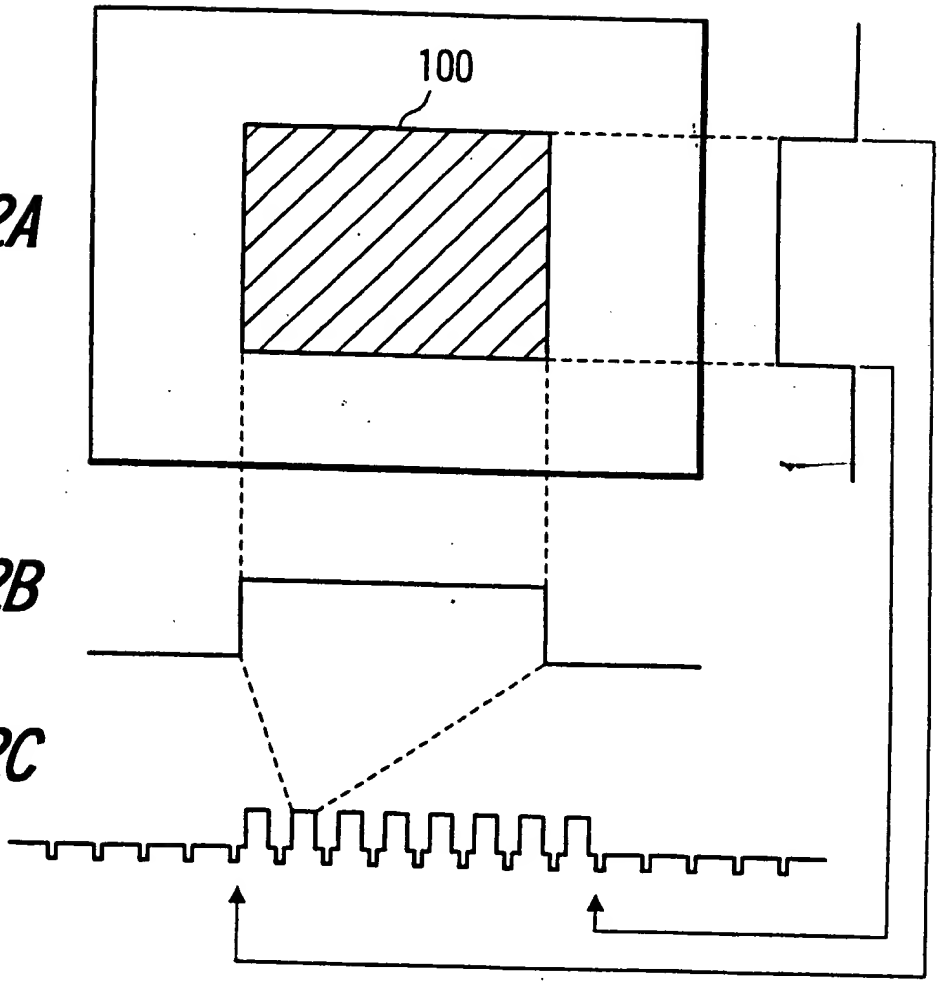


FIG. 3

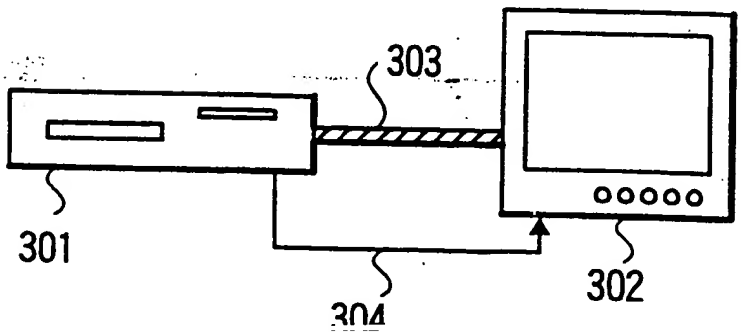
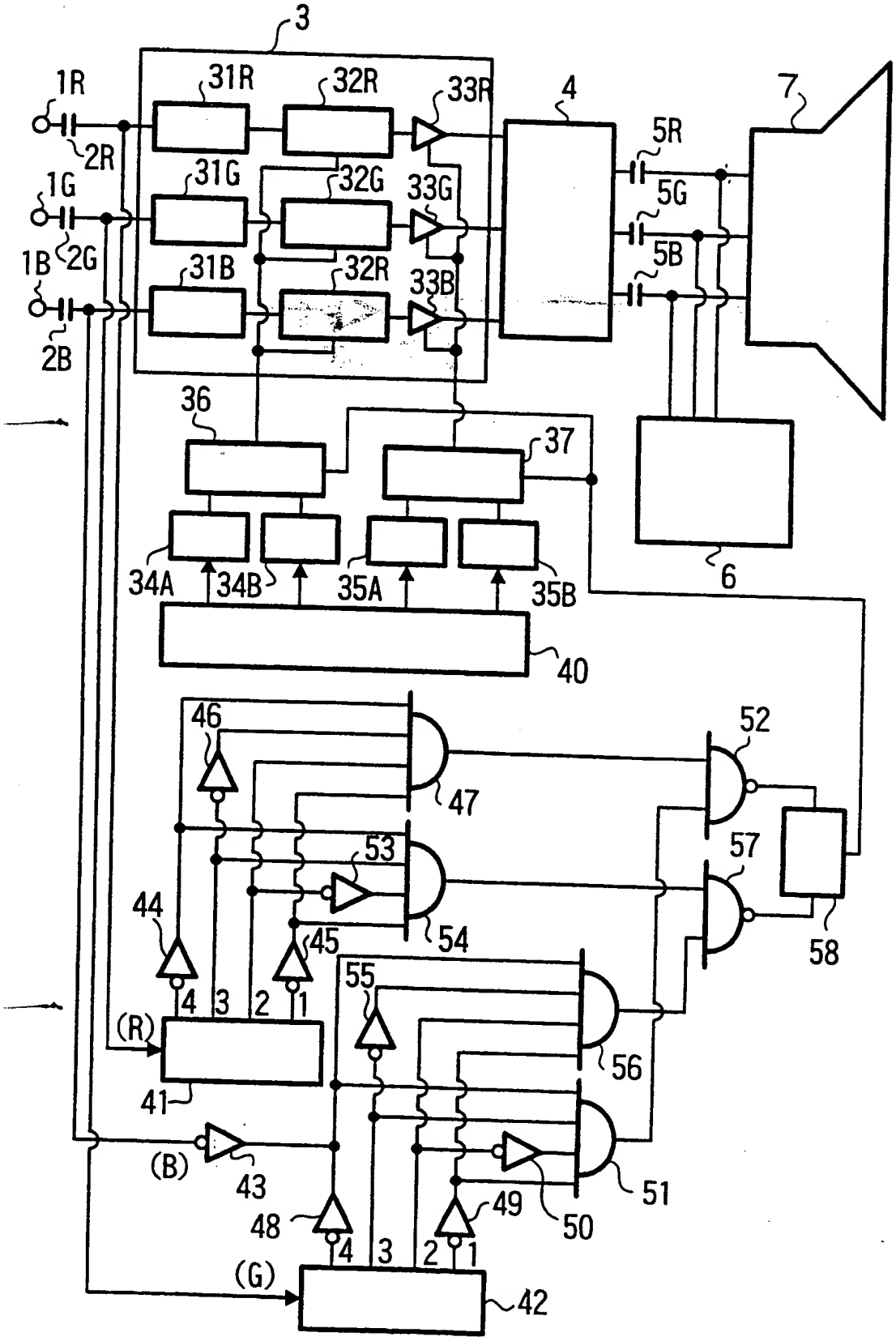


FIG. 4


3
1R
2R
1G
2G
1B
2B
31R
32R
33R
31G
32G
33G
31B
32R
33B
4
5R
5G
5B
7
6
36
37
34A
34B
35A
35B
40
46
47
52
53
54
57
58
44
45
4
3
2
1
(R)
41
55
56
(B)
43
48
49
50
51
(G)
42

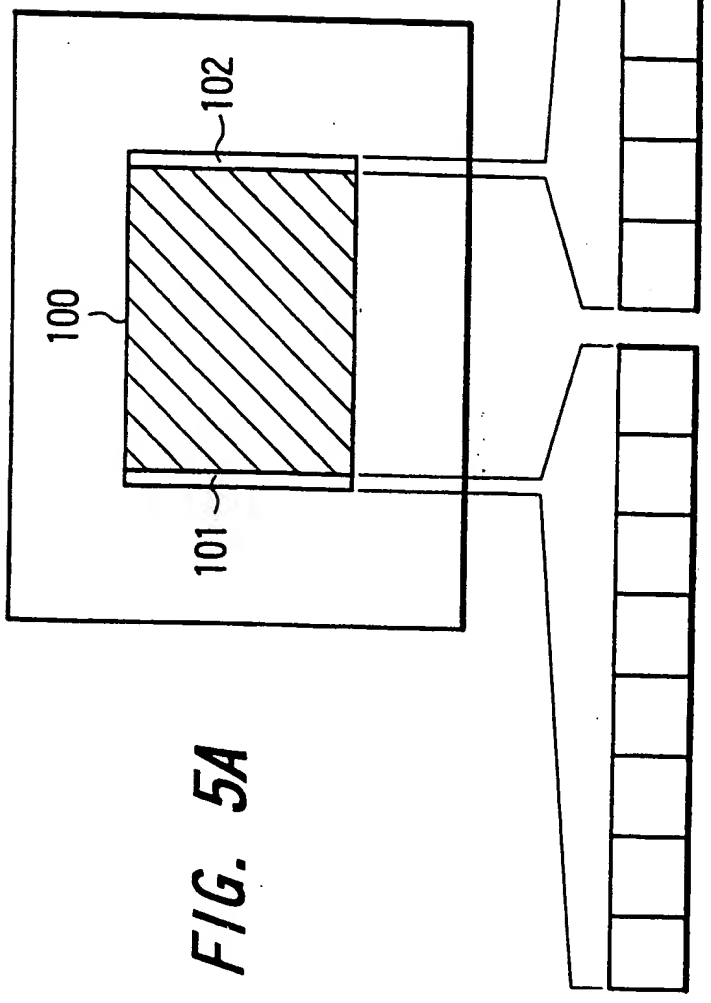


FIG. 5A

FIG. 5B

FIG. 5C

FIG. 6A

FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6E

FIG. 6F

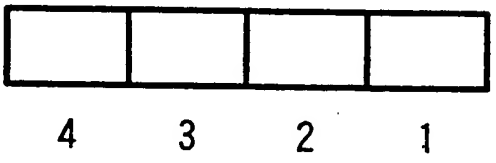


FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

FIG. 7E

FIG. 7F

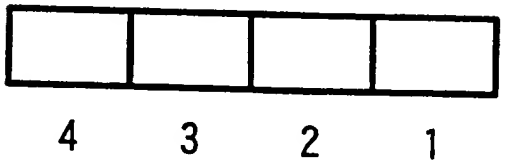


FIG. 8

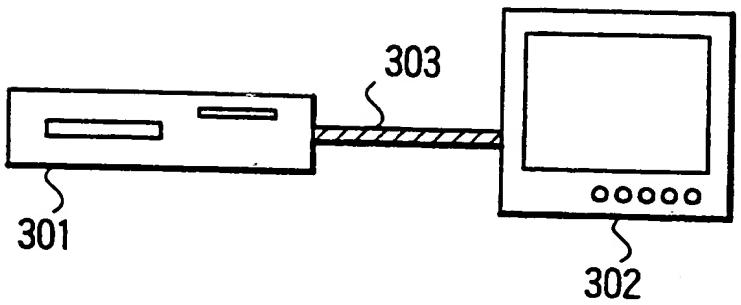


FIG. 9

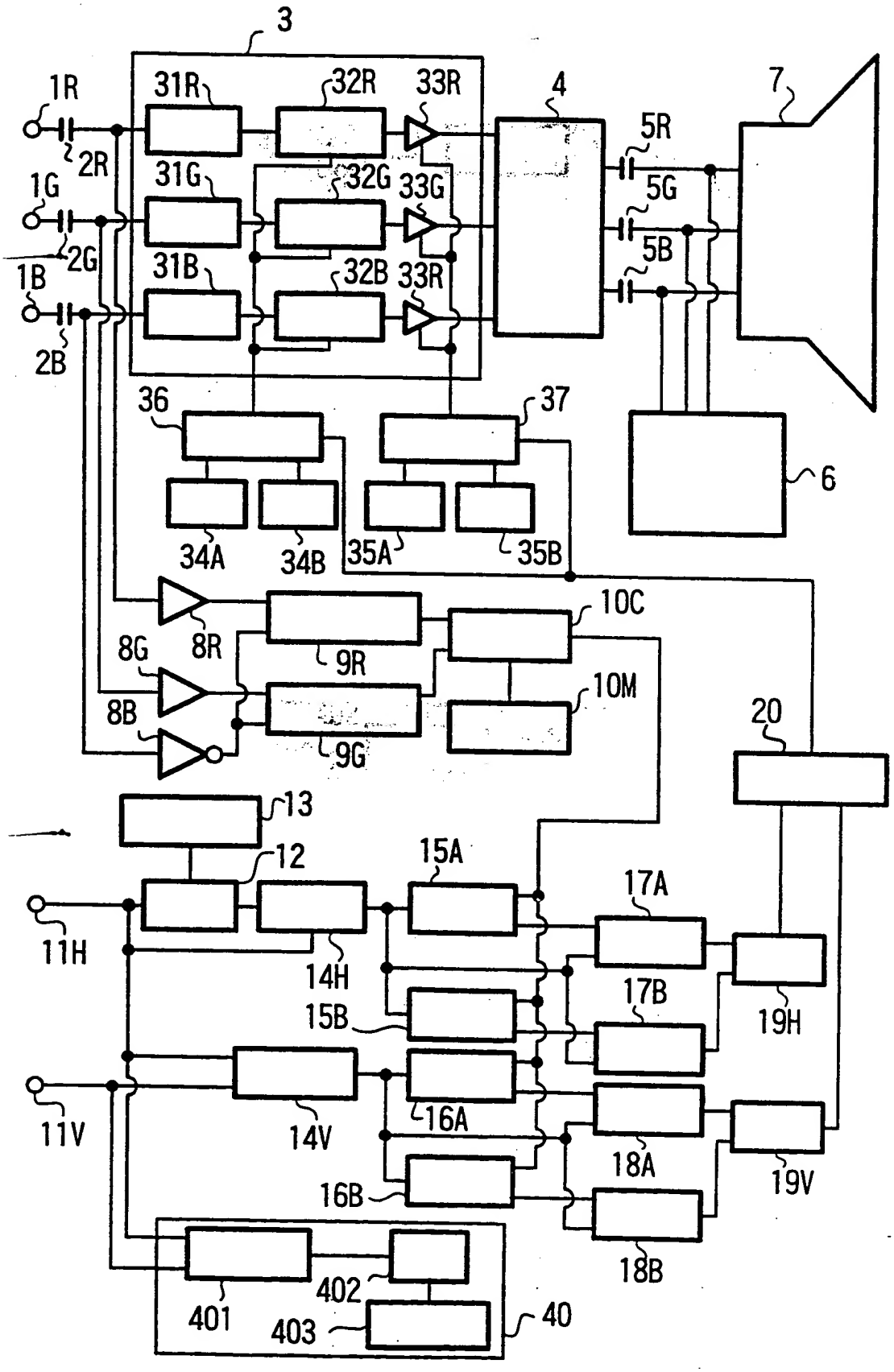

3
1R
2R
1G
2G
1B
2B
31R
32R
33R
31G
32G
33G
31B
32B
33R
4
5R
5G
5B
7
6
36
37
34A
34B
35A
35B
8R
8G
8B
9R
9G
10C
10M
20
13
12
15A
17A
11H
14H
15B
17B
19H
11V
14V
16A
18A
19V
16B
18B
401
402
403
40

FIG. 10A

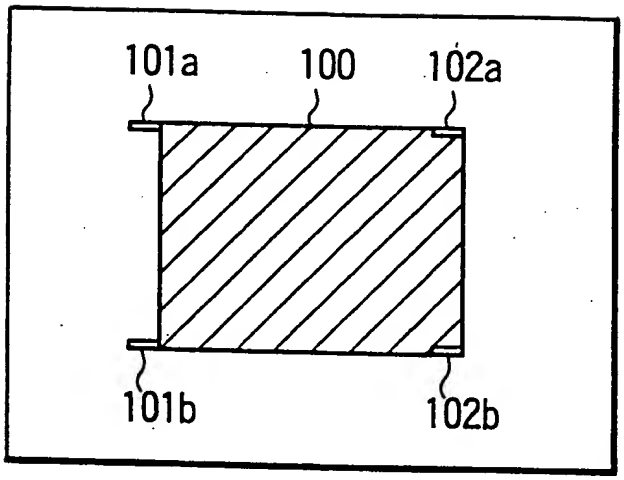


FIG. 10B

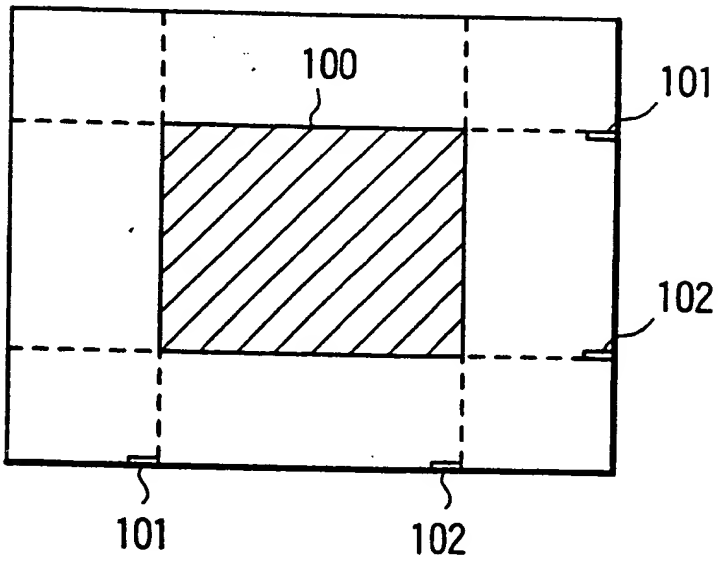


FIG. 11

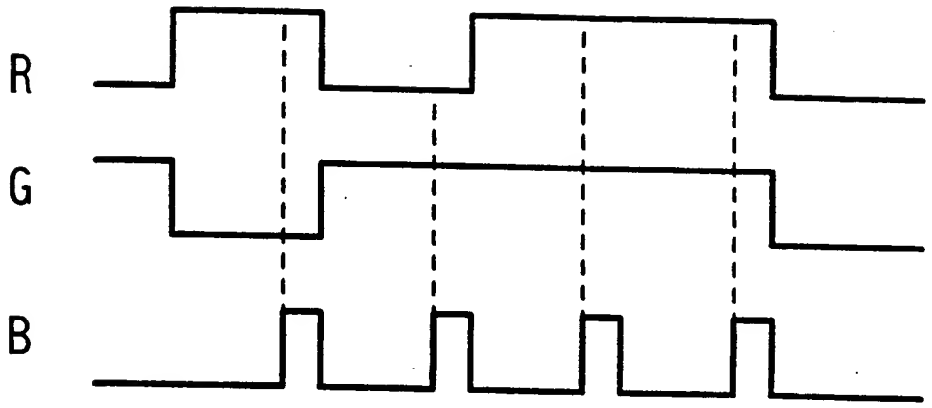


FIG. 12

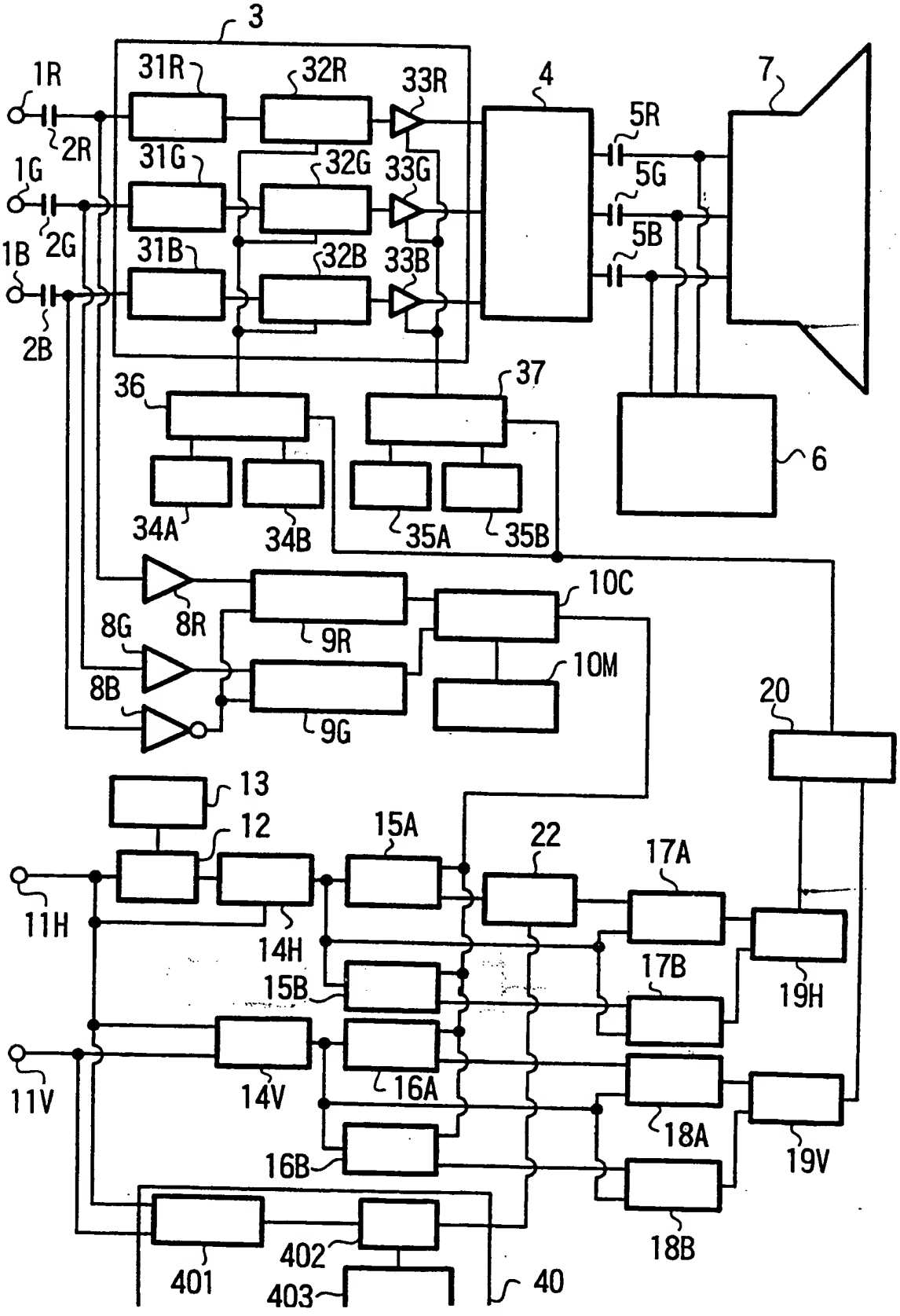

3
1R
2R
1G
2G
1B
2B
31R
32R
33R
31G
32G
33G
31B
32B
33B
4
5R
5G
5B
7
6
36
37
34A
34B
35A
35B
8R
8G
8B
9R
9G
10C
10M
20
13
12
15A
22
17A
11H
14H
15B
17B
19H
11V
14V
16A
18A
19V
16B
18B
401
402
403
40

FIG. 13

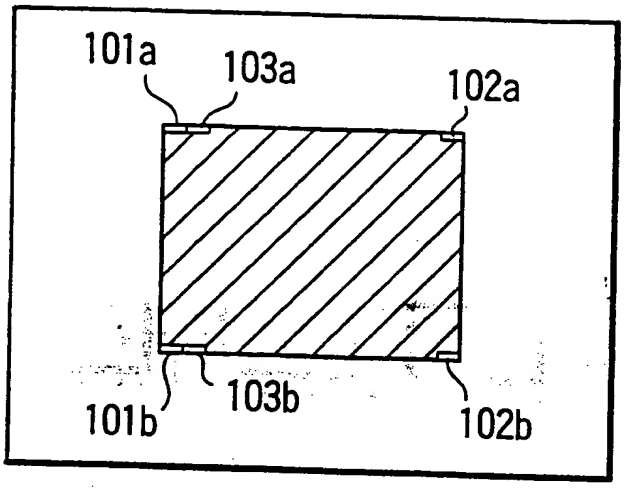


FIG. 14

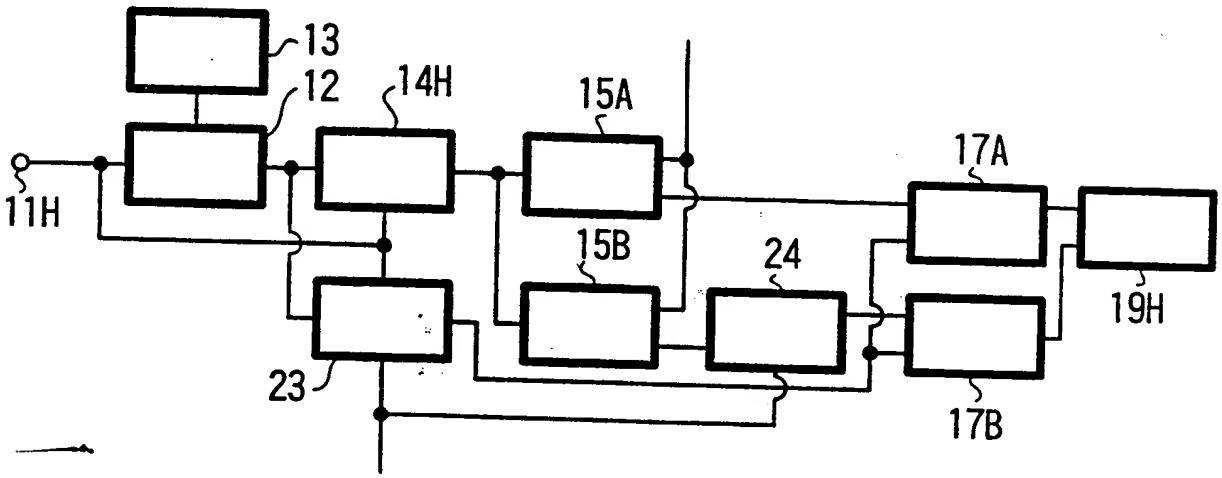


FIG. 15

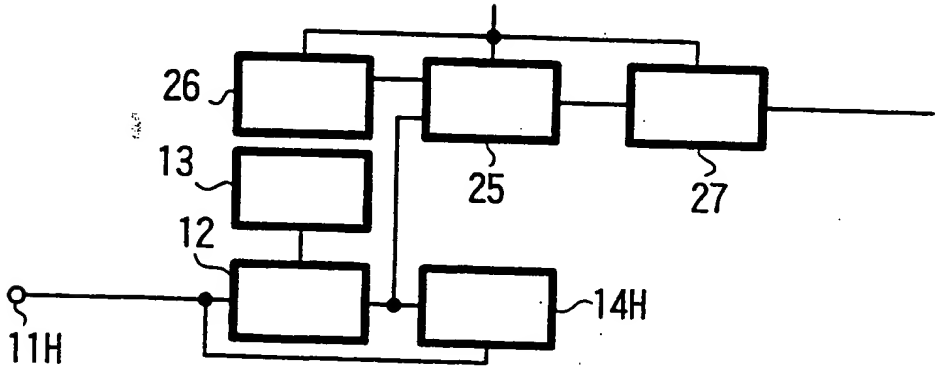


FIG. 16

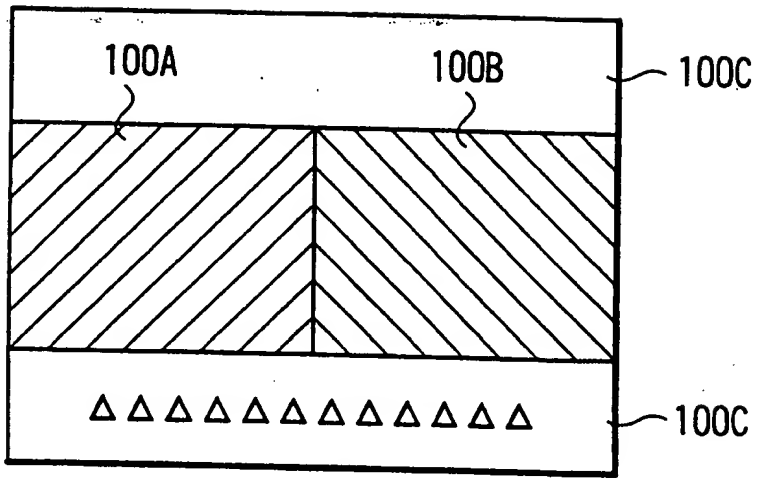
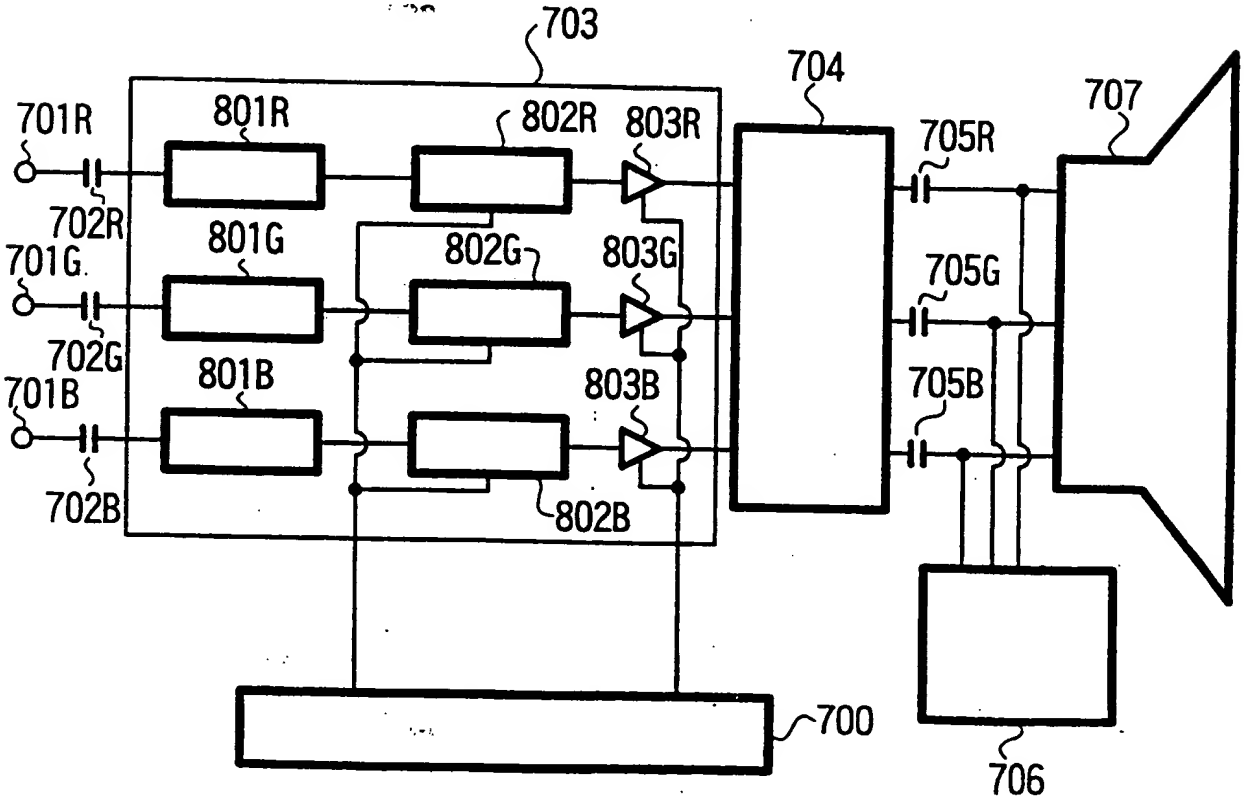

100A
100B
100C
100C

FIG. 17


703
704
707
701R
801R
802R
803R
705R
702R
801G
802G
803G
705G
701G
702G
801B
803B
705B
701B
702B
802B
700
706

符号及び事項の一覧表

符号	事項
1R，1G，1B	入出力端子
2R，2G，2B	コンデンサ
3	プリアンプＩＣ
31R，31G，31B	クランプ回路
32R，32G，32B	シャープネス改善回路
33R，33G，33B	増幅器
34A，34B，35A，35B	Ｄ／Ａ変換回路
37，37	スイッチ回路
38	制御端子
4	出力アンプ
5R，5G，5B	コンデンサ
6	カットオフ調整アンプ
7	陰極線管
40	マイクロコンピュータ

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/04747

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] H04N5/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] H04N5/14-5/217, H04N5/38-5/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1998 Jitsuyo Shinan Toroku Koho 1996-1998
Kokai Jitsuyo Shinan Koho 1971-1998

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP, 63-189086, A (NEC Home Electronics Ltd.), 4 August, 1988 (04. 08. 88) (Family: none)	1, 2 3-15
X A	JP, 61-182389, A (Hitachi,Ltd.), 15 August, 1986 (15. 08. 86) (Family: none)	1, 2 3-15
X	JP, 9-139865, A (Matsushita Electric Industrial Co., Ltd.), 27 May, 1997 (27. 05. 97) (Family: none)	15
X	JP, 8-251503, A (Hitachi,Ltd.), 27 September, 1996 (27. 09. 96) (Family: none)	15
X	JP, 6-225326, A (Sanyo Electric Co., Ltd.), 12 August, 1994 (12. 08. 94) (Family: none)	15
A	JP, 8-65543, A (Fujitsu General Ltd.), 8 March, 1996 (08. 03. 96) (Family: none)	1-15
A	JP, 1-165268, A (Sharp Corp.), 29 June, 1989 (29. 06. 89) (Family: none)	1-15

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 January, 1999 (12. 01. 99)	26 January, 1999 (26. 01. 99)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/04747

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 63-33073, A (NEC Corp.), 12 February, 1988 (12. 02. 88) (Family: none)	1-15
A	JP, 5-236348, A (Fuji Photo Film Co., Ltd.), 10 September, 1993 (10. 09. 93) (Family: none)	8-14

国際調査報告

国際出願番号　PCT／JP98／04747

A.　発明の属する分野の分類（国際特許分類（IPC））

Int. Cl⁶ H04N5／20

B.　調査を行った分野

調査を行った最小限資料（国際特許分類（IPC））

Int. Cl⁶ H04N5／14　－5／217
Int. Cl⁶ H04N5／38　－5／46

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報　1926－1998年
日本国公開実用新案公報　1971－1998年
日本国実用新案登録公報　1996－1998年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C.　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
X A	JP，63－189086，A（日本電気ホームエレクトロニクス株式会社） 4．8月．1988年（04．08．88）（ファミリーなし）	1，2 3－15
X A	JP，61－182389，A（株式会社日立製作所） 15．8月．1986年（15．08．86）（ファミリーなし）	1，2 3－15
X	JP，9－139865，A（松下電器産業株式会社） 27．5月．1997年（27．05．97）（ファミリーなし）	15

☒ C欄の続きにも文献が列挙されている。　☐ パテントファミリーに関する別紙を参照。

＊　引用文献のカテゴリー
「A」特に関連のある文献ではなく、一般的技術水準を示すもの
「E」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「O」口頭による開示、使用、展示等に言及する文献
「P」国際出願日前で、かつ優先権の主張の基礎となる出願の日の後に公表された文献
「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「&」同一パテントファミリー文献

国際調査を完了した日	国際調査報告の発送日
12．01．99	26.01.99

国際調査機関の名称及びあて先	特許庁審査官（権限のある職員）		
日本国特許庁（ISA／JP） 郵便番号100－8915 東京都千代田区霞が関三丁目4番3号	乾　雅浩　印	5C	9649
	電話番号　03－3581－1101　内線　3510		

C（続き）　関連すると認められる文献

引用文献のカテゴリー＊	引用文献名　及び一部の箇所が関連するときは、その関連する箇所の表示	関連する請求の範囲の番号
X	JP，8－251503，A（株式会社日立製作所） 27．9月．1996年（27．09．96）（ファミリーなし）	15
X	JP，6－225326，A（三洋電機株式会社） 12．8月．1994年（12．08．94）（ファミリーなし）	15
A	JP，8－65543，A（富士通ゼネラル株式会社） 8．3月．1996年（08．03．96）（ファミリーなし）	1－15
A	JP，1－165268，A（シャープ株式会社） 29．6月．1989年（29．06．89）（ファミリーなし）	1－15
A	JP，63－33073，A（日本電気株式会社） 12．2月．1988年（12．02．88）（ファミリーなし）	1－15
A	JP，5－236348，A（富士写真フィルム株式会社） 10．9月．1993年（10．09．93）（ファミリーなし）	8－14

International public disclosure WO 99/21355, April 29, 1999
International application PCT/JP 98/04747, October 20, 1998
Priority (JP) patent application 9-287050, October 20, 1997
(JP) patent application 10-88958, April 1, 1998
Applicant Sony Corp.

54)
57)

Specification.

Display device, marker signal forming method, marker signal detecting circuit, and control signal generating circuit.

Field of technology.

This invention pertains to a display device, marker signal forming method, marker signal detecting circuit, and control signal generating circuit, that are very suitable for use in the case that for instance a display is executed, wherein a screen is split into a number of areas, and in each of these areas images with different image qualities have been formed. This invention particularly pertains to such a display device, marker signal forming method, marker signal detecting circuit, and control signal generating circuit, that in the display of image signals wherein areas that display information such as characters and numerals and areas that introduce and display images such as photographs and moving images, have been established, particularly the image quality of the display of photographs and moving images etc. is improved, without loss of the display of characters and numerals etc.

Background technology.

In display devices such as television receivers, that for instance display image signals that depend on television broadcasting, and image signals that have been played back from video tapes etc., from way back techniques for improvement of the image quality such as for instance enlargement of the difference of luminance of the white level and the black level (below called contrast ratio) of display images by an increase of the rate

of amplification of the image signal, and emphasis on the contour of the image (below called sharpness), are being executed in order to improve the image quality of the display for still standing images, whereof photographs are typical examples, and moving images, whereof movies are typical examples.

Moreover, many kinds of semiconductor integrated circuits (below called IC), that have at least one of such image quality improving functions, and control these image quality improving functions by for instance a control means wherein a direct current voltage (below called DC voltage) from outside, or a means of information transmission such as the so-called bus communication, have been realised. As typical examples thereof, for instance a pre-amplifying IC that is used in the image amplifying circuit, and an RGB decoding IC that decomposes luminance and colour difference signals to red, green and blue signals, etc. are known.

That is to say that figure 17 shows an example of the construction of a display device wherein such an image quality improving function has been established. In order to facilitate the understanding of the results of this invention that will be discussed below, this figure 17 shows the construction of a display device such as a monitor display device that receives and displays signals from for instance a computer, and the explanation of the existing technique is executed for this construction.

In figure 17, for instance red, green and blue image signals (R/G/B) that have been inputted in input terminals 701R, 701G and 701 B, are supplied to pre-amplifying IC 703 via the respective condensors 702R, 702G and 702B. By this pre-amplifying IC 703, the supplied image signals (R/G/B) are respectively supplied to sharpness improving circuits 802R, 802G and 802B, via clamping circuits 801R, 801G and 801B, and then they are produced via amplifiers 803R, 803G and 803B.

Moreover, for instance a sharpness controlling DC voltage and a contrast ratio controlling DC voltage, that are outputted from microcomputer (below called micon) 700, that is present inside the device, and carries out the control of the various functions, are supplied to preamplifying IC 703. Hereby, for instance the sharpness improving circuits 802R, 802G and 802B, and amplifiers 803R, 803G and 803B are controlled by preamplifying

circuit 703, and respectively improvement of sharpness and contrast ratio are executed.

Then the image signals (R/G/B) that are picked up from this preamplifying IC 703, are again amplified by output amplifier 704, and thereafter picked up via condensors 705R, 705G and 705B. Then, these picked up image signals (R/G/B) are submitted to DC voltage conversion in cut-off regulating amplifier 706, and then supplied to for instance cathode ray tube (below called CRT) 707, in the case that this is the display means, and on the tube surface of CRT 707, an image that depends on image signals (R/G/B) with improved image quality is displayed.

Now in for instance a monitor display device that serves to display the output of a computer, hitherto the main aim was to display information such as characters and numerals of documents and table calculations etc., that are outputted from a computer. Therefore, the display of image signals that are supplied from a computer, by for instance the binary signals '1/0', with a proper luminance level, was carried out with the use of a general monitor display device.

In the recent computers that are called multimedia, on the other hand, not only information such as the above mentioned characters and numerals, but also images such as photographs and moving images from disc devices and video cards are displayed in an arbitrary range, that is called a window. In this case, the images such as photographs and moving images that have thus been introduced, have a lower contrast and sharpness than information of characters and numerals, and in the case that these are displayed together, the image quality of photographs and moving images etc. appears as having remarkably deteriorated.

Here, it has been considered to carry out an improvement of the above mentioned contrast ratio and sharpness in such monitor display devices, with the aim to improve the image quality of images such as photographs and moving images.

In existing monitor display devices, however, the improvement of the image quality such as the above mentioned enlargement of the luminance difference and reinforcement of the countour, is uniformly carried out over the screen as a whole. In the case that areas of display of characters and numerals etc. are present in the screen, therefore rather the risk is produced that the display thereof is difficultly readable. The result is that

particularly in the case that the luminance of the display of characters and numerals etc. is too high, this acts as an effect of deterioration of the image quality, such as easy tiring of the eye, and impossibility of observation (use) during a long time.

Moreover, by the development of the so-called internet and the popularity of character broadcasting, recently also in general television receivers the occasions of execution of display of images such as photographs and moving images, and of characters and numerals in one single screen, are increasing. Consequently, also in such television receivers the risk occurs that the display of characters and numerals in the screen becomes difficultly readable when the improvement of the image quality such as the above mentioned enlargement of the luminance difference and the reinforcement of the contour is carried out uniformly over the entire screen.

This application is the result of a study of such points, and the problem that should be solved is that when in existing devices, images such as photographs and moving images are displayed together with information such as characters and numerals, the image quality of images such as photographs and moving images is found to have remarkably deteriorated, and that, when improvement of the image quality of these photographs and moving images etc. is carried out, the image quality of the display of characters and numerals etc. deteriorates.

Disclosure of the invention.

In this invention, arbitrary areas of the screen that is displayed are designated, and in each of these designated areas, an arbitrary image processing is executed, and hereby, it is made possible to improve the image quality of images such as photographs and moving images without making information such as characters and numerals difficult to discern, in the case that images such as photographs and moving images are displayed, together with information such as characters and numerals, and connected herewith, the display device, the method of marker signal construction, the circuit of marker signal detection and the control signal generating circuit of this invention are disclosed.

Brief description of the figures.

Figure 1 is a drawing of the construction that shows an example of the display device of the first situation of execution of this invention.

Figure 2 is a figure for the explanation thereof.

Figure 3 is a figure of the construction of the whole thereof.

Figure 4 is a drawing of the consctruction that shows an example of the display device of the second situation of execution of this invention.

Figure 5 is a drawing of the consctruction that shows an example of the display device of the third situation of execution of this invention.

Figure 6 is a figure for the explanation thereof.

Figure 7 is a figure for the explanation thereof.

Figure 8 is a figure of the construction of the whole thereof.

Figure 9 is a drawing of the construction of an example of the marker signal detecting circuit of the fourth situation of execution of this invention.

Figure 10 is a figure for the explanation thereof.

Figure 11 is an explanatory drawing of another example of the method of marker signal construction of the third situation of execution of this invention.

Figure 12 is a drawing of the construction that shows an example of the control signal generating circuit of the fifth situation of execution of this invention.

Figure 13 is a figure for the explanation thereof.

Figure 14 is a drawing of the construction that shows another example of the control signal generating circuit of the fifth situation of execution of this invention.

Figure 15 is a drawing of the construction that shows an example of the control signal generating circuit of the sixth situation of execution of this invention.

Figure 16 is a drawing for the explanation of the display device of the seventh situation of execution of this invention.

Figure 17 is a drawing for the explanation of an existing device.

Optimum situation for the execution of this invention.

Below, in the explanation of this invention, referring to figures, figure 1 is a block diagram that shows the construction of an example of a monitor display device wherein the display device of the first situation of execution of this invention has been used.

In this figure 1, for instance the red, green and blue image signals (R/G/B) that have been inputted in input terminals 1R, 1G and 1B, are supplied to preamplifying IC 3, respectively via condensors 2R, 2G and 2B. By this preamplifying IC 3, the supplied image signals (R/G/B) are respectively supplied to sharpness improving circuits 32R, 32G and 32B, that will be discussed below, via clamping circuits 31R/31G and 31B, and then they are produced via amplifiers 33R, 33G and 33B, that will be discussed below.

The image signals (R/G/B), that have been produced from this preamplifying IC 3, are then amplified by output amplifier 4, and thereafter produced via condensors 5R, 5G and 5B. Then these produced image signals (R/G/B) are submitted to DC voltage conversion in cut-off regulating amplifier 6, and then supplied to for instance cathode ray tube (below called CRT) 7, in the case that it is the display means, and on the tube surface of CRT 7, an image that depends on the image signals (R/G/B) with improved image quality, that will be discussed below, is displayed.

Moreover, by microcomputer (below called micon) 40, that is present inside this device and that carries out control of the various functions, for instance data of the first and second DC voltage that carry out the control of the above mentioned sharpness, and data of the first and second DC voltage that carry out control of the contrast ratio, are formed. Then these data that have been formed are respectively supplied to D/A converter (below called DAC) circuits 34A and 34B, and 35A and 35B, and respectively converted to the control DC voltage.

Now the control DC voltages that have been converted by these DAC circuits 34A and 34B, and 35A and 35B, are respectively selected by switching circuits 36 and 37, and supplied to the above mentioned preamplifying IC 3. Hereby, for instance the above mentioned sharpness improving circuits 32R, 32G and 32B, and amplifiers 33R, 33G and 33B are controlled by preamplifying IC 3, according to the control DC voltages that have been sup-

plied, and improvement of respectively sharpness and contrast ratio is carried out.

In this device, then control signals that designate arbitrary areas of the screen that is displayed, are supplied to control terminal 38, for instance from an external computer (not shown in the figure). For these control signals, here a pulse signal that corresponds with the width in horizontal direction of area 100 as is shown in figure 2B, and a pulse signal that corresponds with the width in vertical direction, as is shown in figure 2C, are synthetized for instance for arbitrary area 100 on the display screen, as is shown in figure 2A, and the control signal as is shown in figure 2D, is formed.

Now the control signal from this terminal 38 is supplied to the above mentioned switching circuits 36 and 37, and converted by the above mentioned DAC circuits 34A and 34B, and 35A and 35B and selection of the thus obtained control DC voltage is carried out. Moreover, the control DC voltage that has been selected by these switching circuits 36 and 37, is supplied to above mentioned pre-amplifying IC 3. In the image that is displayed in above mentioned CRT 7, hereby, the sharpness and contrast ratio of the image in the designated arbitrary area are changed by the above mentioned control signal.

That is to say that in this device, it is possible to raise only the sharpness and contrast ratio in the area of image 100 such as a photograph or moving image that have been introduced in for instance a display screen, more than in other sections, and that hereby, the image quality of area 100 of the image such as a photograph or moving image that have been introduced, can be improved. In the above mentioned explanation, the horizontal synchronism signal in the control signal of figure 2 is one that has been added for the convenience of the explanation, and there are also cases wherein it is not present in the actual signal.

By the fact that in this device an arbitrary area of the screen is designated, and only in this area the arbitrary image processing is carried out, it is consequently possible to improve the image quality of images that have been introduced, without hampering the visibility of information such as characters and numerals, in the case that introduced images such as photographs and moving images and information such as characters and numerals are displayed together.

Hereby, cases that in the existing device had the problem that in the case that introduced images and information such as characters and numerals were displayed together, they appeared as cases wherein the image quality of photographs and moving images etc. had remarkbly deteriorated, are cases wherein such problems can be solved in a simple way by this invention.

In the above mentioned explanation, the situation was adopted that the image quality is improved by for instance raising sharpness and contrast ratio of only the area of images such as photographs and moving images more than in other sections, but it is also posible to use other means that improve the image quality, by gamma correction and colour correction etc.

Now in the above mentioned first situation of execution, it is necessary to connect special line 304 for the above mentioned control signals in addition to cable 303 for the image signal, for instance between personal computer 301 and monitor display device 302, as is for instance shown in figure 3. This special line 304 for control signals can for instance use an empty channel of cable 303 for image signals, but anyhow, a signal line is occupied.

On the other hand, the second situation of execution of this invention is one wherein the signal that designates the above mentioned arbitrary area of the screen, is supplied, superimposed on the image signal. That is to say that figure 4 is a block diagram that shows the construction of an example of a monitor display device wherein the display device of the second situation of execution of this invention has been used. In this figure 4, sections that correspond with above mentioned figure 1, have got the same symbols, and a double explanation is omitted.

In this figure 4, an image signal (R/G/B) whereon a marker signal, that designates the above mentioned arbitrary area of the screen, has been superimposed, is for instance supplied from a computer (not shown in the figure) as the parent machine, to input terminals 1R, 1G and 1B. Herein, prescribed signal patterns 101 and 102, that are marker signals, are established in this image signal, in both end sections of the horizontal direction of arbitrary area 100 that is designated, continuing in vertical direction, as is for instance shown in figure 5A.

Moreover, for this marker signal, for instance for signal

pattern 101 at the starting side (left) of the horizontal direction, various colour signals in the order blue, black, blue, red, blue, green, blue, black, as is shown in figure 5B, have been establshed in the form of stripes. Moreover, in signal pattern 102 at the finishing end (right) of the horizontal direction, various colour signals in the order blue, black, blue, green, blue, red, blue, black, as is shown in figure 5C, are established in the form of stripes.

That is to say that in this construction, the third situation of execution of this invention is the method of construction of marker signals with the characteristic that signals wherein primary colour signals with prescribed levels have respectively been combined with an arbitrary pattern, are established in the image signal, and that the pattern of one primary colour signal is used as the clock, and that the marker code is formed by the pattern of the other primary colour signals.

Herein, the image signals from these input terminals 1R, 1G and 1B are supplied to the above mentioned pre-amplifying IC 3, and for instance the red image signal (R) from input terminal 1R is supplied to the input terminal of shift register 41, the green image signal (G) from input terminal 1G is supplied to the input terminal of shift register 42, and the blue image signal (B) from input terminal 1B is supplied to the clock terminals of shift registers 41 and 42 via inverter 43.

Consequently, when in these shift registers 41 and 42, for instance signal pattern 101 of the starting side (left) of the horizontal direction as is shown in figure 6A, is supplied, the descent of the respective blue signals is, as is shown in figure 6B, delayed a little, and a clock is supplied. By the descent of the first blue signal, thus a signal for the timing of the first black signal is introduced, as is shown in figure 6C.

Moreover, by the descent of the second blue signal, a timing signal for the red signal is introduced, as is shown in figure 6D. Moreover, by the descent of the third blue signal, a timing signal for the green signal is introduced, as is shown in figure 6E. Moreover, by the descent of the fourth blue signal, a timing signal for the final black signal is introduced, as is shown in figure 6F. These signals are successively shifted to the right.

On the other hand, in above mentioned shift registers 41 and 42, the respective red image signals (R) are supplied to shift

register 41, and the green signals (G) are supplied to shift register 42. In the situation that the timing signal of the above mentioned final black signal has been introduced (figure 6F), therefore in shift register 41 the signal is introduced from the second bit, and in shift register 42, the signal is introduced from the third bit.

By the fact that here, in above mentioned figure 4, the signal of the second bit of this shift register 41 and the signal wherein the other bits have been inverted (inverters 44, 45 and 46), are supplied to AND circuit 47, and the signal of the third bit of shift register 42 and the signal wherein the other bits have been inverted (inverters 48, 49 and 50), are supplied to AND circuit 51, and the outputs of these AND circuits 47 and 51 are supplied to NAND circuit 52, signal pattern 101 of the starting side (left) of the horizontal direction is detected.

In the same way, a clock is supplied by a little delay after the descent of the respective blue signals, as is shown in figure 7B, when signal pattern 102 at the final side (right) of the horizontal direction, as is for instance shown in figure 7A, is supplied to shift registers 41 and 42. By the descent of the initial blue signal, the timing signal of the initial black signal is introduced, as is shown in figure 7C.

Moreover, by the descent of the second blue signal, the timing signal of the green signal is introduced, as is shown in figure 7D. Moreover, by the descent of the third blue signal, the timing signal of the red signal is introduced, as is shown in figure 7E. Moreover, by the descent of the fourth blue signal, the timing signal of the final black signal is introduced, as is shown in figure 7F. Moreover, these signals are successively shifted to the right.

In the above mentioned shift registers 41 and 42, on the other hand, respectively the red image signals (R) are supplied to shift register 41, and the green image signals (G) are supplied to shift register 42. In the situation that the timing signal of the above mentioned final black signal has been introduced (figure 7F), therefore a signal from the second bit is introduced in shift register 41, and a signal from the third bit is introduced in shift register 42.

By the fact that here, as is shown in figure 4, the signal of the third bit of this shift register 41 and the signal wherein

the other bits have been inverted (inverters 44, 45 and 53), are supplied to AND circuit 54, and the signal of the second bit of shift register 42 and the signal wherein the other bits have been inverted (inverters 48, 49 and 55), are supplied to AND circuit 56, and the outputs of these AND circuits 54 and 56 are supplied to NAND circuit 57, signal pattern 102 of the finishing side (right) of horizontal direction is detected.

Then, the output of above mentioned NAND circuit 52 is supplied to setting (S) terminal of flipflop 58, and the output of above mentioned NAND circuit 57 is supplied to resetting (R) terminal of flipflop 58. In the Q output of this flipflop 58, hereby a discrimination signal that corresponds with the period from detection of above mentioned signal pattern 101 at the starting side (left) of the horizontal direction to the detection of the signal at the finishing side (right), is introduced.

This introduced discrimination signal is supplied to above mentioned switching circuits 36 and 37, and selection of the control DC voltage, that has been converted by the above mentioned DAC circuits 34A and 34B, and 35A and 35B, is carried out. The control DC voltage that has been selected by these switching circuits 36 and 37, is supplied to above mentioned preamplifying IC 3. Hereby, the sharpness and contrast ratio of the image in the arbitrary area that has been designated by the above mentioned control signal, are changed.

That is to say that in this device, it is possible to raise sharpness and contrast ratio only in area 100 of images such as photographs and moving images, that have been introduced in for instance the display screen, to a higher level than in other parts, and that hereby, the image quality of area 100 of introduced images such as photographs and moving images can be improved. These improvements of image qualities can also be executed by gamma correction and colour correction etc.

Consequently, also in this device it is possible to improve the image quality of introduced images without hampering the visibility of information such as characters and numerals, in the case that introduced images such as photographs and moving images, and information such as characters and numerals are displayed together, by execution of the arbitrary image processing only in this area.

Hereby, cases that had the problem that they appeared as cas-

es with a remarkably reduced image quality such as photographs and moving images in the case that introduced images and information such as characters and numerals were displayed together in the existing device, are cases wherein the problems can be solved in a simple way by this invention.

Moreover, in the second situation of execution, it is possible to improve the image quality of introduced photographs and moving images etc., by simply connecting cable 303 for image signals, for instance between personal computer 301 and monitor display device 302, as is for instance shown in figure 8.

Moreover, as the third situation of execution of this invention, detection of the marker code can be carried out in a simple and reliable way by establishing a signal wherein primary colour signals with the prescribed level have been combined with an arbitrary pattern, in the image signal, and by forming a marker code, with the pattern of one primary colour signal as the clock, by the pattern of the other primary colour signals.

Moreover, in figure 9, the construction of another example wherein a marker signal detecting circuit has been used, as the fourth situation of execution, in a monitor display device wherein the display device of the above mentioned second situation of execution has been adopted, is shown. In the explanation of figure 9, parts that correspond with above mentioned figure 4 have got the same symbols, and a double explanation is omitted.

That is to say that in this figure 9, as is for instance shown in figure 10A, the same signal patterns 101a and 101b at the starting side (left) and signal patterns 102a and 102b at the finishing side (right) of the horizontal direction as in above mentioned figure 5, are for instance established for each horizontal period, as marker signals, in sections that correspond with the four corners of arbitrary area 100 on the display screen.

In this figure 9, the horizontal synchronism signal from input terminal 11H is suppied to PLL circuit 12, and to this PLL circuit 12, the oscillation signal from oscillator 13 is supplied, and an arbitrary clock signal that has been synchronised with the horizontal synchronism signal, is formed. This clock signal is supplied to the counting terminal of horizontal counter 4H, and the horizontal synchronism signal or a signal that has been synchronized with the horizontal synchronism signal are

supplied to the resetting terminal. Hereby, a counting value that corresponds with the horizontal position on the display screen, is produced from this horizontal counter 14H.

Moreover, the horizontal synchronism signal is supplied to the counting terminal of vertical counter 14V, and the vertical synchronism signal from input terminal 11V or a signal that has been synchronized with the vertical synchronism signal are supplied to the resetting terminal. Hereby, the counting value that corresponds with the vertical position on the display screen is produced from this vertical counter 14V. Then, the counting values of these horizontal counter 14H and vertical counter 14V are supplied to respectively latching circuits 15A and 15B, and 16A and 16B.

Moreover, via amplifiers 8R and 8G, the image signals from above mentioned input terminals 1R and 1G are supplied to the input terminals of shift registers 9R and 9G, and via comparator 8B, the image signal from input terminal 1B is supplied to the clock terminal of shift registers 9R and 9G. Then the signals that have been accumulated in these shift registers 9R and 9G are supplied to comparator 10C, and compared with signal patterns 101 or 102, that for instance have been memorized in memory 10M.

Also hereby, the detection of signal patterns 101 and 102 can be carried out in the same way as in the circuit of NAND circuits 52 and 57, from shift registers 41 and 42 in above mentioned figure 4. Moreover, in this section, the circuit of NAND circuits 52 and 57 may also be established from shift registers 41 and 42. The detection signal of signal patterns 101 and 102, that has been detected by this comparator 10C or NAND circuits 52 and 57, is supplied to the trigger terminal of respectively latching circuits 15A and 16A, and 15B and 16B.

In latching circuit 15A, hereby the counting value that corresponds with the horizontal position of for instance signal pattern 101a or 101b on the display screen is latched. Moreover, in latching circuit 15B, the counting value that corresponds with the horizontal position of for instance signal patterns 102a or 102b on the display screen is latched.

Moroever, in latching circuit 16A, the counting value that corresponds with the vertical position of for instance signal pattern 101a or 102a on the display screen is latched. Moreover,

This Page Blank (uspto)

in latching circuit 16B, the counting value that corresponds with the vertical position of for instance signal pattern 101b or 102b on the display screen is latched.

Here, the signals that have been latched in these latching circuits 15A and 15B, and 16A and 16B, are supplied to respectively comparators 17A and 17B, and 18A and 18B, and the counting values of above mentioned horizontal counter 14H and vertical counter 14V are supplied to respectively comparators 17A and 17B, and 18A and 18B.

From comparator 17A, hereby a signal is produced when the counting value of horizontal counter 14H coincides with the counting value of the horizontal position of signal patterns 101a or 101b that have been latched in latching circuit 15A. Moreover, from comparator 17B, a signal is produced when the counting value of horizontal counter 14H coincides with the counting value of the horizontal position of signal patterns 102a or 102b that have been latched in latching circuit 15B.

Moreover, from comparator 18A, a signal is produced when the counting value of vertical counter 14V coincides with the counting value of the vertical position of signal patterns 101a or 102a that have been latched in latching circuit 16A. Moreover, from comparator 18B, a signal is produced when the counting value of vertical counter 14V coincides with the counting value of the vertical position of signal patterns 101b or 102b that have been latched in latching circuit 16B.

By the fact that these signals from comparators 17A and 17B are supplied to the setting and resetting terminals of flipflop 19H, a pulse signal that corresponds with the amplitude in horizontal direction of the same area 100 as was shown in above mentioned figure 2B, is produced. Moreover, by the fact that the signals from comparators 18A and 18A (should this be 18B? translator) are supplied to the setting and resetting terminals of flipflop 19V, a pulse signal that corresponds with the amplitude in vertical direction of the same area 100 as was shown in above mentioned figure 2C, is produced.

Moreover, by the fact that the signals from these flipflops 19H and 19V are synthetised by(?) multiplier 20, the same control signal as is shown in for instance above mentioned figure 2D, is formed. This control signal is supplied to above mentioned switching circuits 36 and 37, and converted by DAC circuits

34A or 34B and 35A or 35B, and by carrying out selection of the thus obtained control DC voltage, the sharpness and contrast ratio of the image of the arbitrary area that has been designated by the above mentioned control signal in the image that is displayed in above mentioned CRT 7, are changed.

That is to say that in this device, it is possible to raise the sharpness and contrast ratio of only area 100 of images such as for instance photographs and moving images, that have been introduced in the display screen, more than that of other sections, and that hereby, the image quality of area 100 of the introduced images such as photographs and moving images can be improved. This improvement of image quality can also be carried out by gamma correction and colour correction.

Consequently, also in this device it is possible to improve the image quality of introduced images, without hampering the visibility of information such as characters and numerals, in the case that introduced images such as photographs and moving images are displayed together with information such as characters and numerals, by the fact that an arbitrary area of the screen is designated, and an arbitrary image processing is carried out only in this area.

Then, as the fourth situation of execution of this invention, the detection of the marker code can be carried out in a simple and reliable way by the fact that it has been equipped with a first memory that, with the timing of a clock that depends on one primary colour signal, takes in a pattern of the other primary colour signals, and a second memory wherein a pattern of the other primary colour signals that form a marker code, have been memorized in advance, and a means of comparison that successively causes shifting of the pattern that has been taken in in the first memory and compares it with the pattern that has been memorized in the second memory.

Also in this example, it is possible to improve the image quality of introduced photographs and moving images etc., by simply connecting cable 303 for image signals, between for instance personal computer 301 and monitor display device 302, as is for instance shown in figure 8.

Moreover, in the above mentioned example of figure 9, it is possible to carry out processing also in the case that for instance at the side of the computer, a cursor etc. has been form-

ed, superimposed on signal patterns 101a, 102a, 101b and 102b. That is to say that in the case that in the above mentioned device a cursor etc. has been formed, superimposed on a signal pattern, at the side of the computer, this signal pattern can no longer be detected with above mentioned circuit 40.

According to the example of above mentioned figure 9, however, one of the signal patterns 101a and 101b may be detected for the starting end of the horizontal direction, and one of the signal patterns 102a and 102b may be detected for the finishing end, and by the detection of one thereof, processing is carried out. In the same way one of the signal patterns 101a and 102a, or signal patterns 101b and 102b may be detected for the upper and lower end of the vertical direction, and by the detection of one thereof, processing is carried out.

In the above mentioned device, consequently processing can also be carried out in the case that for instance a cursor etc. has been formed, superimposed on a signal pattern, at the side of the computer. Moreover, the cursor is smaller than the designated area 100, and it is not thought that such a cursor is simultaneously piled upon two or more signal patterns. Or in the case that there is no risk that such a cursor is completely piled on the signal pattern, for instance the left lower signal pattern 102b may be cancelled.

Moreover, in the above mentioned device, it is also possible to carry out processing after establishment of signal patterns 101 and 102 on the continued line of starting and finishing end of the horizontal direction and upper and lower end of the vertical direction of area 100, as is for instance shown in figure 10B. In this case, also the risk of piling of the cursor on the signal pattern is widely reduced by the fact that for instance the position wherein signal patterns 101 and 102 are established, is outside the display screen.

Moreover, in the above mentioned device, it is possible to create the situation that a number of areas can be designated on the display screen, by establishing a number of sets of signal patterns 101 and 102, that are the marker signals, with respectively the same or different patterns. By carrying out the same or different image processings for these numbers of designated areas, it is possible to carry out the optimum improvement of image quality in the respective images, for a screen wherein im-

ages with various image qualities have been combined.

Moreover, figure 11 shows the construction of another example of the method of construction of a marker signal as the third situation of execution of this invention. That is to say that in figure 11, for instance the blue (B) signal in the primary colour signals is used as the clock, and that the marker signal is constructed with the red (R) and green (G) signals. With the timing of the ascent of the blue (B) signal (descent of the inverted signal), the pattern of red (R) and green (G) signals is for instance introduced in above mentioned shift registers 9R and 9G.

That is to say that in the example that is shown in the figure, for instance pattern (1011) is introduced in shift register 9R, and pattern (0111) in shift register 9G. By comparison of these patterns with the pattern that has been memorized in memory 10M, for instance the signal patterns 101 and 102, that are the arbitrary marker signals, are detected. The construction of the signal that is shown in the figure, is an example, and by for instance changing the above mentioned pattern, and increasing or decreasing the number of bits, a number of kinds of signal patterns can be constructed.

Moreover, in the example of figure 11, a signal is constructed in such a way that the timing of the clock that for instance depends on the blue (B) signal, and the points of change of the patterns of the red (R) and green (G) signals do not coincide. Hereby, the detection of the signal patterns (reading into the shift register) can be carried out in a stable way.

Moreover, in the construction of the device of above mentioned figure 9, for instance the blue (B) signal is supplied to the clock terminal of shift registers 9R and 9G, via comparator 8B. Hereby, the situation is produced that for instance a small delay is produced in the timing of the clock that depends on the blue (B) signal.

In image signals wherein black and white patterns, such as for instance characters and numerals, are alternately produced, hereby white is detected in a relaible way, also in cases wherein, by the above mentioned delay, there was the risk of detection of random signals and false detection of the arbitrary pattern by the influence of time shifting of the red (R) and green (G) signals, for instance in the edge section of the blue (B)

signal, and it is possible to eliminate the risk of false detection of a pattern , for instance by not using a pattern with a full section '1'.

Now, the reason that in above mentioned figures 10A and 10B, the signal pattern has been placed at the front side in the horizontal direction of area 100, is that the detection of the signal pattern, as is shown in above mentioned figures 6 and 7, is carried out with a final black timing, but this can be freely corrected by establishment of a means that corrects the timing.

Here, in addition figure 12 shows the construction of a control signal generating circuit, that carries out correction of the position of the above mentioned signal pattern, as the fifth situation of execution of this invention. In this figure 12, an example of the case of application in the monitor display device, wherein the display device of the above mentioned second situation of execution was used, is shown. Moreover, in the explanation of this figure 12, parts that correspond with the above mentioned figure 4, have got the same symbols, and a double explanation is omitted.

In this figure 12, horizontal and vertical synchronism signals that are supplied to above mentioned input terminals 11H and 11V, are to supplied to in-built timer 401 of microcomputer 40, and the frequencies of the horizontal and vertical synchronism signals are determined. Then these determined frequencies of the horizontal and vertical synchronism signals are supplied to central processing unit (below called CPU) 402, and the length of time of the signal pattern that constitutes the above mentioned marker signal, is obtained from data that have been memorized in for instance memory 403.

Then the value of the count of the horizontal clock signal that corresponds with the obtained time length, is calculated by CPU 402. Then this calculated value is supplied from microcomputer 40 to subtractor 22, that has for instance been established in the output of latching circuit 15A. Hereby, the position of the marker signal that has for instance been memorized in latching circuit 15A, can be shifted over a part of the above obtained time length, at the front side of the horizontal direction.

That is to say that hereby, as is for instance shown in figure 13, the signal patterns 101a and 101b, that constitute the

marker signal, can be established inside area 100, that is detected by the marker signal. Hereby, for instance signal patterns 101a and 101b that constitute the marker signal, can be formed without protrusing outside area 100, and establishment of area 100 can be facilitated.

Moreover, figure 14 shows another example of the construction of the control signal generating circuit, as the fifth situation of execution of this invention. In this figure 14, only the essential parts are shown, and other parts are the same as the construction of figure 12.

In this figure 14, for instance counter 23, that simultaneously carries out the counting of above mentioned horizontal counter 14H, is established. In this counter 23, position correcting data that correspond with the time length from above mentioned computer 40 (not shown in the figure), are pre-loaded, and the count value of this counter 23 is supplied to comparators 17A and 17B. In addition, adder 24 is established in the output of latching circuit 15B, and by this adder 24, the above mentioned position correcting data are added.

That is to say that in this case, the position of the display screen is shifted relatively more to the rear side, and that by the addition of position correcting data in the output of latching circuit 15B, detection of domain 100 can be carried out by signal patterns 101a, 101b, 102a and 102b, that have been established inside area 100. In this case, the scale of the circuit as a whole can be reduced by the fact that it is constructed with an adder, and that no subtractor is used.

As the sixth situation of execution of this invention, a further correction of the position of the signal pattern can well be executed in the above mentioned control signal generating circuit, by addition of a code that allows determination of the time length of the above mentioned signal pattern, to the marker signal. That is to say that in above mentioned figure 13, for instance arbitrary signal patterns (codes) 103a and 103b, that show the end of the pattern, are added, in succession to signal patterns 101a and 101b, that constitute the marker signal.

In the case that here determinations are carried out with the use of these signal patterns 103a and 103b, execution is possible as is for instance shown in figure 15. That is to say that in figure 15, for instance counter 25 that simultaneously car-

ries out the count of above mentioned horizontal counter 14H, is established. In addition, also for instance flipflop 26, that is set/reset by the detection signals of signal patterns 101a and 101b, and 103a and 103b, is established, and by the output of this flipflop 26, the count of counter 25 is controlled.

Hereby, the count value that for instance corresponds with the time from the finishing end of signal patterns 101a and 101b to the finsihing end of signal patterns 103a and 103b, is produced from counter 25. By establishing here the position of signal patterns 103a and 103b in such a way that this time is the time length of signal patterns 101a and 101b, the time length of the above mentioned signal patterns can be determined. Then this count value is established in latching circuit 27, and the same correction of the position of the signal pattern as mentioned above can be carried out.

That is to say that in this case, the time length of the signal pattern can be determined, and the position of the signal pattern can be corrected, without the use of microcomputer 40.

Moreover, for instance in the case that image signals that are supplied to input terminals 1R, 1G and 1B, are generated by a parent computer (not shown in the figure), the processing that establishes such a signal pattern, is, at the side of this parent computer (not shown in the figure), carried out with only addition of for instance software, and no processing in the hardware sense is necessary. Consequently, it is possible to use the above mentioned device wherein this invention has been applied, connected with a freely chosen multi-purpose computer etc.

Moreover, also in the case that image signals wherein such signal patterns have been established, are recorded in a recording medium such as a video tape or video disc, and such recording media are played back and displayed, this above mentioned invention can be used.

Moreover, according to the above mentioned device, it is not necessary that the user carries out any operation in the above mentioned processing, and the processing is automatically carried out, and for instance also in the case that area 100 has been shifted and that the size has been changed, the changes of the position and size can be followed.

Moreover, the seventh situatioh of execution of this inven-

tion is a display device wherein a number of image signals are inputted, and these image signals are respectively displayed in windows, and in each of these windows and other areas, wherein these image signals are displayed, different image processings can be carried out.

That is to say for instance in a television receiver, the synthesis and display of a number of inputted image signals is, as is for instance shown in figure 16, carried out in the respective windows 100A and 100B. Moreover, in some cases for instance characters and numerals (ΔΔΔΔ) are displayed in window 100C, wherein such an image signal is not synthetized.

By the fact that in such a television receiver, different image processings are carried out in each of the windows 100A, 100B and 100C, it is possible to improve the image quality of the introduced image without hampering the visibility of information such as for instance characters and numerals. In this case, detection of windows 100A, 100B and 100C etc. can for instance be carried out by an internal synthesis circuit of the television receivcer, and it is not necessary to establish special marker signals for the detection.

When then it is a display device to display images according to the display device of the first situation of execution of this invention, it is possible to improve the image quality of introduced photographs and moving images etc., without hampering the visibility of information such as characters and numerals, by establishing a control signal that designates arbitrary areas of the screen that is displayed, and establishing an image processing means that executes the respective arbitrary image processings in each of these designated areas, based on the control signal.

Moreover, when it is a display device for display of images according to the second situation of execution of this invention, it is possible to improve the image quality of introduced photographs and moving images etc., without hampering the visibility of information such as characters and numerals, by supplying the image signal whereto a marker signal has been attached, in an arbitrary area of the screen that is displayed, and establishing an image processing means that detects the marker signal and carries out different image processings in each area wherein it has been detected.

Moreover, according to the method of construction of the marker signal of the third situation of execution of this invention, detection of the marker code can be carried out in a simple and reliable way by establishing a signal wherein the primary colour signals with the respective prescribed levels have been combined with an arbitrary pattern in the image signal, using the pattern of one primary colour signal as the clock, and forming a marker code with the pattern of the other primary colour signals.

Moreover, according to the marker signal detecting circuit of the fourth situation of execution of this invention, it is possible to carry out detection of the marker code in a simple and reliable way by establishing a signal wherein the primary colour signals with the respective prescribed levels have been combined with an arbitrary pattern in the image signal, using the pattern of one primary colour signal as the clock, and forming a marker code with the pattern of the other primary colour signals, providing a first memory that takes in the pattern of the other primary colour signals with the timing of the clock that depends on the pattern of one primary colour signal, for at least the marker signal that designates the arbitrary area of the screen that is displayed by the image signal, and a second memory wherein the pattern of the other primary colour signals, that forms the marker code, has been memorized in advance, and a means of comparison that compares the pattern that has been taken in in the first memory, while it is successively shifted, with the pattern that has been memorized in the second memory.

Moreover, according to the control signal generating circuit of the fifth situation of execution of this invention, it is possible to form the signal pattern that constitutes the marker signal, without protrusion thereof outside the area, and it is possible to facilitate establishment of the area, by establishing a signal wherein the primary colour signals with the respective prescribed levels have been combined with an arbitrary pattern in the image signal, using the pattern of one primary colour signal as the clock, and forming a marker code with the pattern of the other primary colour signals, and providing a detection means that detects the marker signal for at least the marker signal that designates the arbitray area of the screen that is displayed by the image signal, and a determining means that

determines the frequencies of the horizontal and vertical synchronism signals of the image signal, and a processing means that obtains the time length of the marker signal from the determined frequencies of the horizontal and vertical synchronism signals, and a correcting means that corrects the horizontal position of the marker signal with the use of the obtained time length.

Moreover, according to the control signal generating circuit of the sixth situation of execution of this invention, it is possible to form the signal pattern that constitutes the marker signal without protrusion outside the area, and it is possible to facilitate the establishement of the area, by establishing a signal wherein the primary colour signals with the respective prescribed levels have been combined with an arbitrary pattern in the image signal, using the pattern of one primary colour signal as the clock, and forming a marker code with the pattern of the other primary colour signals, and providing a detection means that detects the marker signal for at least the marker signal that designates the arbitrary area of the screen that is displayed by the image signal, and wherein at least a code that allows determination of the length has been attached to the marker signal that is established at the starting end of the horizontal direction of the area, and a processing means that obtains the time length of the marker signal with the use of the code that allows determination of the length, and a correcting means that corrects the horizontal position of the marker signal with the use of the obtained time length.

Moreover, according to the seventh situation of execution of this invention, it is possible to improve the image quality of introduced images without hampering the visibility of information such as characters and numerals, by being a display device wherein a number of image signals are inputted, and the number of image signals are respectively displayed in windows, and by establishing an image processing means that executes different image processings in each of the windows and other areas wherein a number of image signals are displayed.

This invention is not limited to the above explained situations of execution, and various forms are possible, without violation of the essentials of this invention.

What is claimed.

1. A display device with the characteristic that

it is a display device for the display of images,

that a control signal that designates an arbitrary area of the above mentioned screen that is displayed,

and that an image processing means that carries out the respective arbitrary image processings in each of these designated areas, based on the above mentioned control signal, is established.

2. A display device with the characteristic that in the display device that has been described in claim 1,

the above mentioned image processing means freely carries out at least one or more image processings such as contour correction, luminance correction, gamma correction, and colour correction, for each of the images in the above mentioned designated areas.

3. An image display device with the characteristic that

it is a display device for the display of images,

that image signals whereto a marker signal has been added, are supplied to an arbitrary area of the above mentioned screen that is displayed,

and that an image processing means that detects the above mentioned marker signal and carries out different image processings in each of these areas wherein they have been detected, is established.

4. A display device with the characteristic that in the display device that has been described in claim 3,

the above mentioned image processing means freely carries out at least one or more image processings such as contour correction, luminance correction, gamma correction, and colour correction, for each of the images in the above mentioned areas wherein they have been detected.

5. A display device with the characteristic that in the display device that has been described in claim 3,

for the above mentioned marker signal, a prescribed signal pattern is established in both ends of the horizontal direction of the above mentioned arbitrary area, continuing in the vertical direction,

and that an arbitrary image processing is carried out in the

periods between detection of the above mentioned marker signal.

6. A display device with the characteristic that in the display device that has been described in claim 3,

for the above mentioned marker signal, a prescribed signal pattern is established in a section that corresponds with the four corners of the above mentioned arbitrary area,

that two of the above mentioned marker signals that are separated in horizontal direction, are detected, and the area in horizontal direction of the above mentioned arbitrary area is memorized,

and that an arbitrary image processing is carried out, following the above mentioned memorized area in horizontal direction in the period between detection of the two above mentioned marker signals that are separated in vertical direction.

7. A display device with the characteristic that in the display device that has been described in claim 3,

a number of sets are established for the above mentioned marker signals,

and that an image processing means that detects the above mentioned marker signals per set, and carries out diffferent images processings in each area wherein they have been detected, is established.

8. A method of marker signal construction with the characteristic that

a signal wherein primary colour signals with a prescribed level are combined with an arbitrary pattern in the image signal,

and that the pattern of one of the above mentioned primary colour signals is used as the clock, and the marker code is formed with the pattern of the other above mentioned primary colour signals.

9. A method of marker signal construction wherein, in the method of marker signal construction that has been described in claim 8,

it is constructed with a shifting of the timing of the clock that depends on the above mentioned pattern of one primary colour signal, and the points of change of the pattern of the other above mentioned primary colour signals.

10. A method of marker signal construction wherein, in the method of marker signal construction that has been described in

Page Blank (uspto)

claim 8,

in the case that the arbitrary area of the screen that is displayed by the above mentioned image signal, is designated by the above mentioned marker signal,

at least to the above mentioned marker signal that is established in the starting end in horizontal direction of the above mentioned area, a code that allows the determination of its length is added

11. A marker signal detecting circuit that, for a marker signal wherein a signal wherein primary colour signals with prescribed levels have been combined with an arbitrary pattern in the image signal, is established, the pattern of one above mentioned primary colour signal is used as the clock and a marker code is formed by the pattern of the other above mentioned primary colour signals, and that at least designates the arbitrary area of the screen that is displayed by the above mentioned image signal, has been equipped with

a first memory that, with the timing if a clock that depends on the above mentioned pattern of one primary colour signal, takes in the pattern of the other above mentioned primary colour signals,

and a second memory wherein the pattern of the other above mentioned other primary colour signals that form the above mentioned marker code, has been memorized in advance,

and a means of comparison that, under successive shifting of the pattern that has been introduced in the above mentioned first memory, compares it with the pattern that has been memorized in the above mentioned second memory.

12. A marker signal detecting circuit with the characteristic that in the marker signal detecting circuit that has been described in claim 11,

a prescribed delay means for detection of the timing of the clock that depends on the above mentioned pattern of one primary colour signal, in the intake of the pattern of the other above mentioned primary colour signals, is established.

13. A control signal generating circuit that, for a marker signal, wherein a signal wherein primary colour signals with prescribed levels have been combined with an arbitrary pattern in the image signal, is established, the pattern of one above mentioned primary colour signal is used as the clock and a mark-

er code is formed by the pattern of the other above mentioned primary colour signals, and that at least designates the arbitrary area of the screen that is displayed by the above mentioned image signal, has been equipped with

a detection means that detects the above mentioned marker signal,

and a means of determination that determines the frequency of the horizontal and vertical synchronism signals of the above mentioned image signal,

and a processing means that obtains the time length of the above mentioned marker signal from the above mentioned determined frequencies of the horizontal and vertical synchronism signals,

and a correction means that corrects the horizontal position of the above mentioned marker signal with the use of the above mentioned obtained time length.

14. A control signal generating circuit that, for a marker signal wherein a signal wherein primary colour signals with prescribed levels have been combined with an arbitrary pattern in the image signal is established, the pattern of one above mentioned primary colour signal is used as the clock and a marker code is formed by the pattern of the other above mentioned primary colour signals, and that at least designates the arbitrary area of the screen that is displayed by the above mentioned image signal, and a marker signal wherein to the above mentioned marker signal that has been established at least at the starting end in horizontal direction of the above mentioned area, a code that makes it possible to determine its length, has been added, has been equipped with

a detection means that detects the above mentioned marker signal,

and a processing means that obtains the time length of the above mentioned marker signal with the use of the above mentioned code whereby determination of the length is made possible,

and a correction means that corrects the horizontal position of the above mentioned marker signal with the use of the above mentioned obtained time length.

15. A display device with the characteristic that

it is a display device wherein a number of image signals are inputted and the above mentioned number of image signals are

displayed in the respective windows,

and that an image processing means that carries out different image processings in the windows and other areas wherein the above mentioned number of image signals have been displayed.

Figures

List of symbols and items.

symbol	item
1R, 1G, 1B	input terminals
2R, 2G, 2B	condensors
3	preamplifying IC
31R, 31G, 31B	clamping circutis
32R, 32G, 32B	sharpness improving circuit
33R, 33G, 33B	amplifier
34A, 34B, 35A, 35B	D/A conversion circuits
37, 37	switching circuit
38	control terminal
4	output amplifier
5R, 5G, 5B	condensor
6	cut off regulating amplifier
7	cathode ray tube
40	macrocomputer

This Page Blank (uspto)